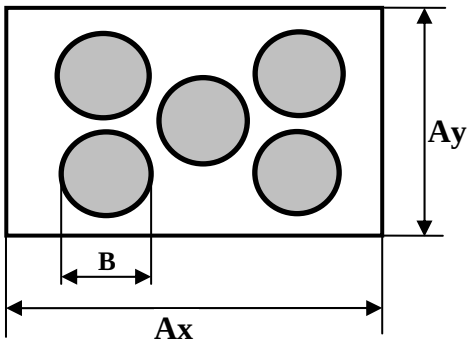
VSP-MIKRON

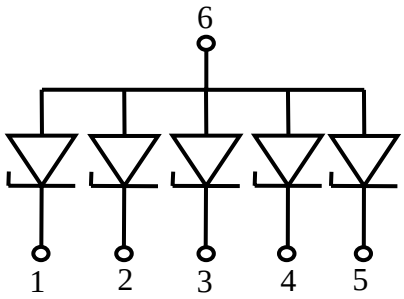
RoHS

Rev.1. March 2010.

KS-5.0V5L1, KS-5.0V5L2

Chip low capacitance 5- fold ESD protection diode.





Schematic and pinning diagram.

Mechanical date: A_x= 480um, A_y=370um, B=90um
Chip thickness: a) 230+/-20um – for KS-5,0V5L1;
b) 138+/-12um – for KS-5,0V5L2.
Scribe Line width - 60um.
Top Metal: Al - for wire bonding, d=2.2+/-0.2 um.
Back side - Anode: Ti-Ni-Ag for soldering.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	t_p=8/20us	25*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	2.5*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15 (Air).	kV
Max.junction temperature	T_j	-	+150	ºC

Characteristics (Tj=25ºC)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	I_R=1mA	6.45	-	7.15	V
I_R	Reverse leakage current	V=5V	-	5	25	nA
V_{CL}	Clamping Voltage	I_{pp}=1.0A, t_p=8/20us I_{pp}=2.5A, t_p=8/20us	-	-	10* 12*	V
C_J	Diode capacitance	V_R=0 V, f =1MHz	-	16	19	pF

*- For Device testing